

TC74ACT299P, TC74ACT299F

8-Bit PIPO Shift Register with Asynchronous Clear

The TC74ACT299 is an advanced high speed CMOS 8-BIT PIPO SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

It has a four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA) controlled by the two selection inputs (S0, S1).

When one or both enable ($\overline{G1}$, $\overline{G2}$) are high, the eight I/O outputs are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

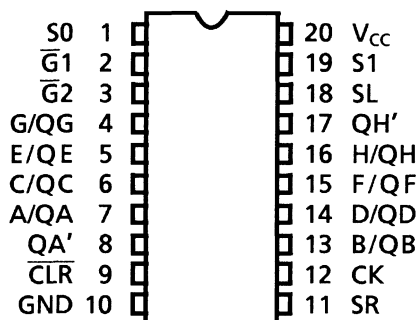
Features (Note 1)(Note 2)

- High speed: $f_{max} = 130$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 8$ μ A (max) at $T_a = 25^\circ$ C
- Compatible with TTL outputs: $V_{IL} = 0.8$ V (max)
 $V_{IH} = 2.0$ V (min)
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 24$ mA (min)
Capability of driving 50 Ω transmission lines.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Pin and function compatible with 74F299

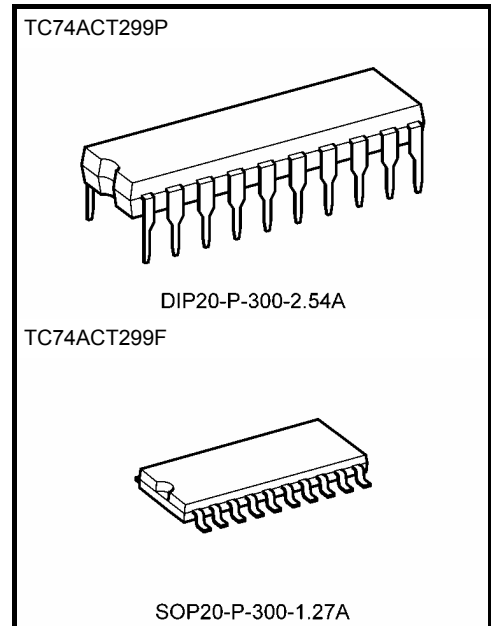
Note 1: Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

Note 2: All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

Pin Assignment

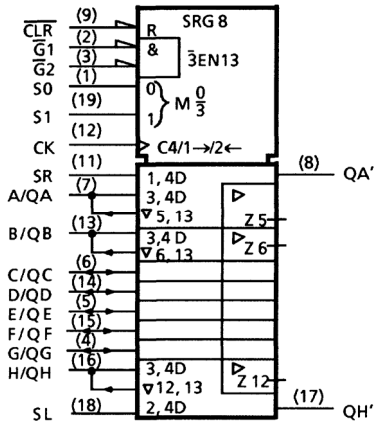


(TOP VIEW)



Weight	
DIP20-P-300-2.54A	: 1.30 g (typ.)
SOP20-P-300-1.27A	: 0.22 g (typ.)

IEC Logic Symbol



Truth Table

Mode	Inputs								Inputs/ Outputs		Outputs	
	CLR	Function Select		Outputs Control		CK	Serial		A/QA	H/QH	QA'	QH'
		S1	S0	G1 (Note)	G2 (Note)		SL	SR				
Z	L	H	H	X	X	X	X	X	Z	Z	L	L
Clear	L	L	X	L	L	X	X	X	L	L	L	L
	L	X	L	L	L	X	X	X	L	L	L	L
Hold	H	L	L	L	L	X	X	X	QA0	QH0	QA0	QH0
Shift	H	L	H	L	L	\uparrow	X	H	H	QGn	H	QGn
Right	H	L	H	L	L	\uparrow	X	L	L	QGn	L	QGn
Shift	H	H	L	L	L	\uparrow	H	X	QBn	H	QBn	H
Left	H	H	L	L	L	\uparrow	L	X	QBn	L	QBn	L
Load	H	H	H	X	X	\uparrow	X	X	a	h	a	h

Note: When one or both output controls are high, the eight input/output terminals are in the high-impedance state; however sequential or clearing of the register is not affected.

Z: High impedance

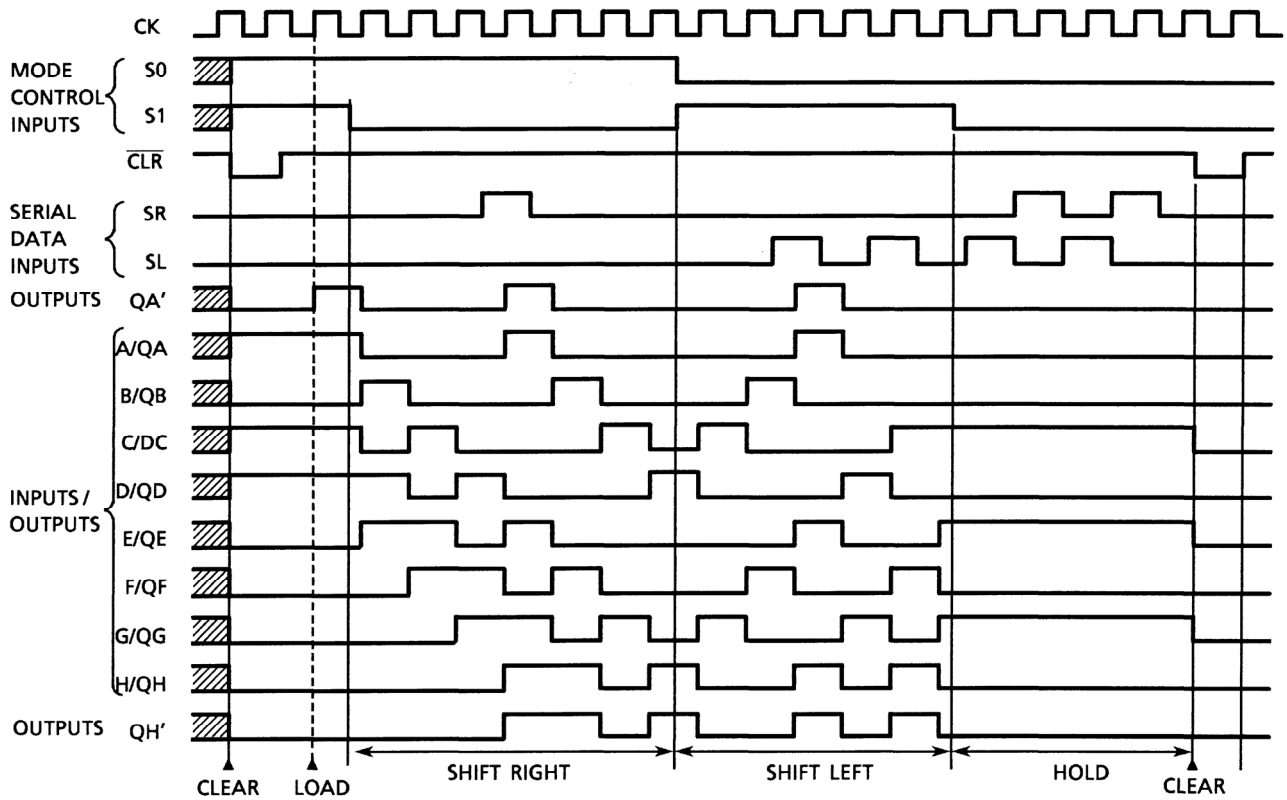
Qn0: The level of Qn before the indicated steady-state input conditions were established.

Qnn: The level of Qn before the most recent active transition indicated by \downarrow or \uparrow .

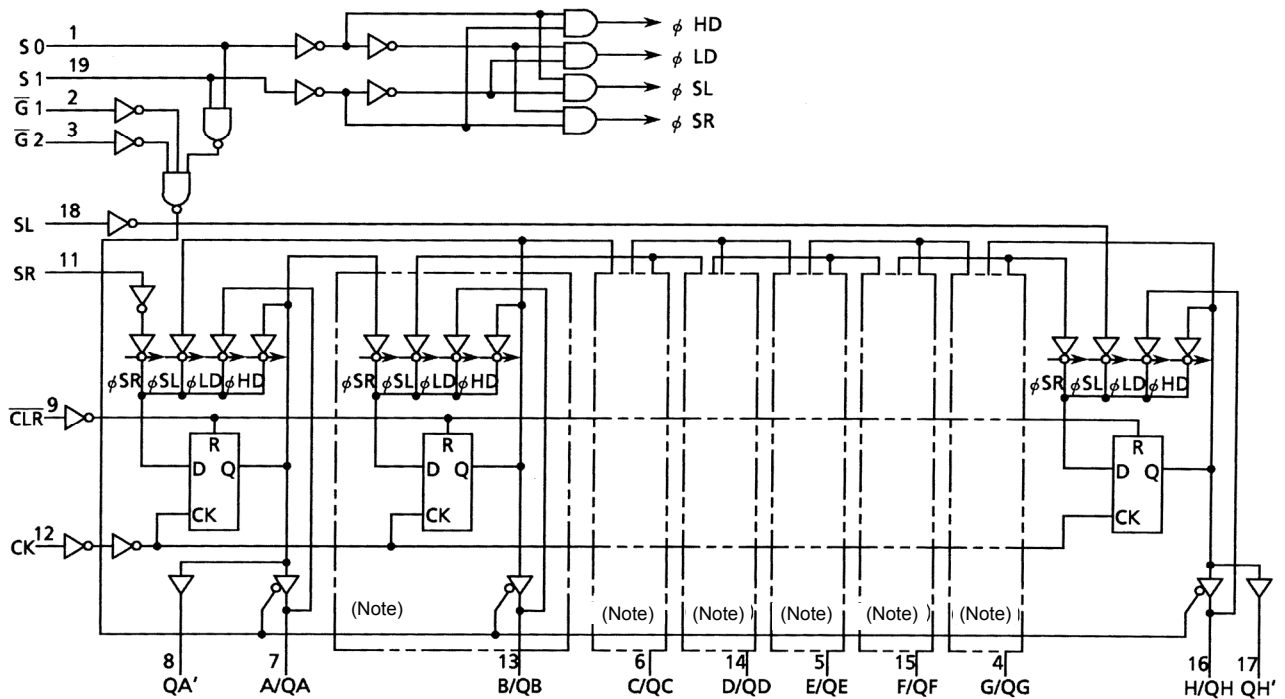
a, h: The level of the steady-state inputs A, H, respectively.

X: Don't care

Timing Chart



System Diagram



Note: Equivalent circuits

Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 50	mA
DC output current	I_{OUT}	± 50	mA
DC V_{CC} /ground current	I_{CC}	± 250	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C a derating factor of -10 mW/°C should be applied up to 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dV	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V _{CC} (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V _{IH}	—		4.5 to 5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V _{IL}	—		4.5 to 5.5	—	—	0.8	—	0.8	V
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	4.5	4.4	4.5	—	4.4	—	V
			I _{OH} = -24 mA	4.5	3.94	—	—	3.80	—	
			I _{OH} = -75 mA (Note)	5.5	—	—	—	3.85	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	4.5	—	0.0	0.1	—	0.1	V
			I _{OL} = 24 mA	4.5	—	—	0.36	—	0.44	
			I _{OL} = 75 mA (Note)	5.5	—	—	—	—	1.65	
3-state output off-state current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	—	—	±0.5	—	±5.0	μA
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	8.0	—	80.0	μA
	I _C	Per input: V _{IN} = 3.4 V Other input: V _{CC} or GND		5.5	—	—	1.35	—	1.5	mA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

Timing Requirements (input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C	Unit	
				V _{CC} (V)	Typ.	Limit		Limit
Minimum pulse width (CK)	t _W (L)	—		5.0 ± 0.5	—	5.0	5.0	ns
	t _W (H)	—						
Minimum pulse width ($\overline{\text{CLR}}$)	t _W (L)	—		5.0 ± 0.5	—	5.0	5.0	ns
Minimum set-up time (SL, SR, A~H)	t _s	—		5.0 ± 0.5	—	3.5	3.5	ns
Minimum set-up time (S0, S1)	t _s	—		5.0 ± 0.5	—	6.0	6.5	ns
Minimum hold time (SL, SR, A~H)	t _h	—		5.0 ± 0.5	—	2.0	2.0	ns
Minimum hold time (S0, S1)	t _h	—		5.0 ± 0.5	—	0.0	0.0	ns
Minimum removal time ($\overline{\text{CLR}}$)	t _{rem}	—		5.0 ± 0.5	—	2.0	2.0	ns

AC Characteristics ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit	
			V _{CC} (V)	Min	Typ.	Max	Min		Max
Propagation delay time (CK-QA', QH')	t _{pLH} t _{pHL}	—	5.0 ± 0.5	—	7.2	10.5	1.0	12.0	ns
Propagation delay time ($\overline{\text{CLR}}$ -QA', QH')	t _{pHL}	—	5.0 ± 0.5	—	6.0	10.0	1.0	11.5	ns
Propagation delay time (CK-QA~QH)	t _{pLH} t _{pHL}	—	5.0 ± 0.5	—	7.4	11.4	1.0	13.0	ns
Propagation delay time ($\overline{\text{CLR}}$ -QA~QH)	t _{pHL}	—	5.0 ± 0.5	—	6.3	10.5	1.0	12.0	ns
Output enable time	t _{pZL} t _{pZH}	—	5.0 ± 0.5	—	7.4	11.4	1.0	13.0	ns
Output disable time	t _{pLZ} t _{pHZ}	—	5.0 ± 0.5	—	7.2	9.6	1.0	11.0	ns
Maximum clock frequency	f _{max}	—	5.0 ± 0.5	80	120	—	80	—	MHz
Input capacitance	C _{IN}	—	—	—	5	10	—	10	pF
Bus input capacitance	C _{I/O}	—	—	—	13	—	—	—	pF
Power dissipation capacitance	C _{PD} (Note)	—	—	—	160	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

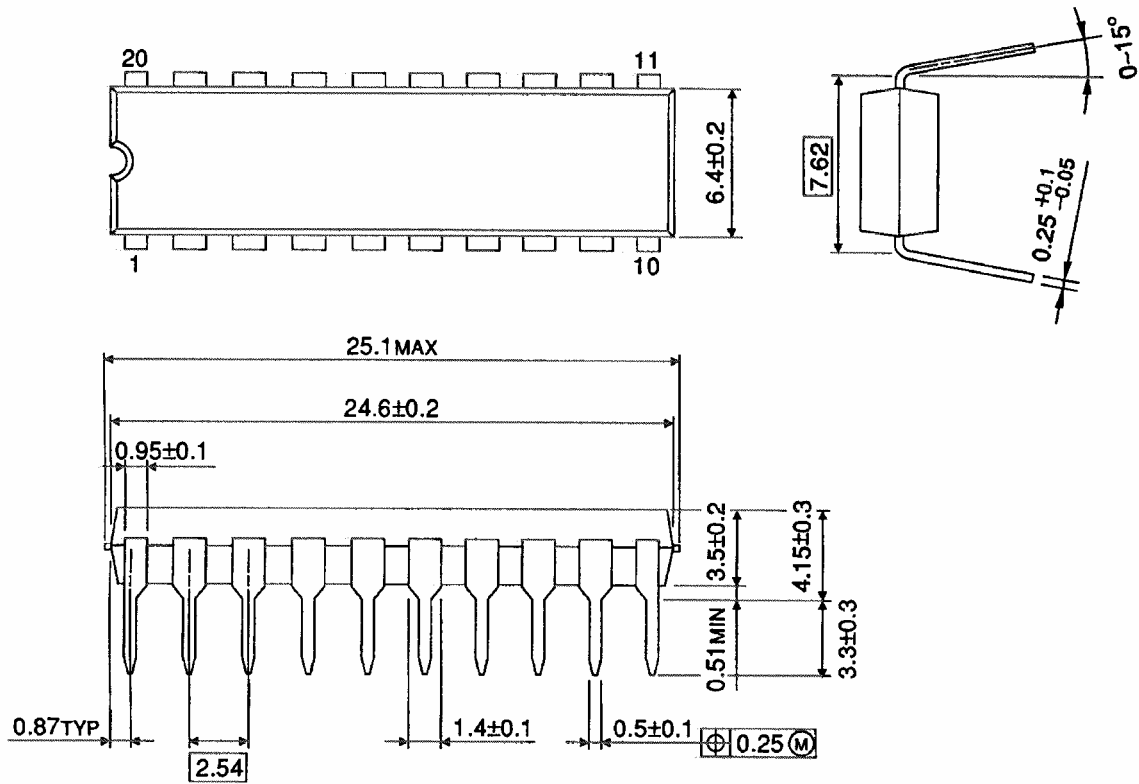
Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions

DIP20-P-300-2.54A

Unit : mm

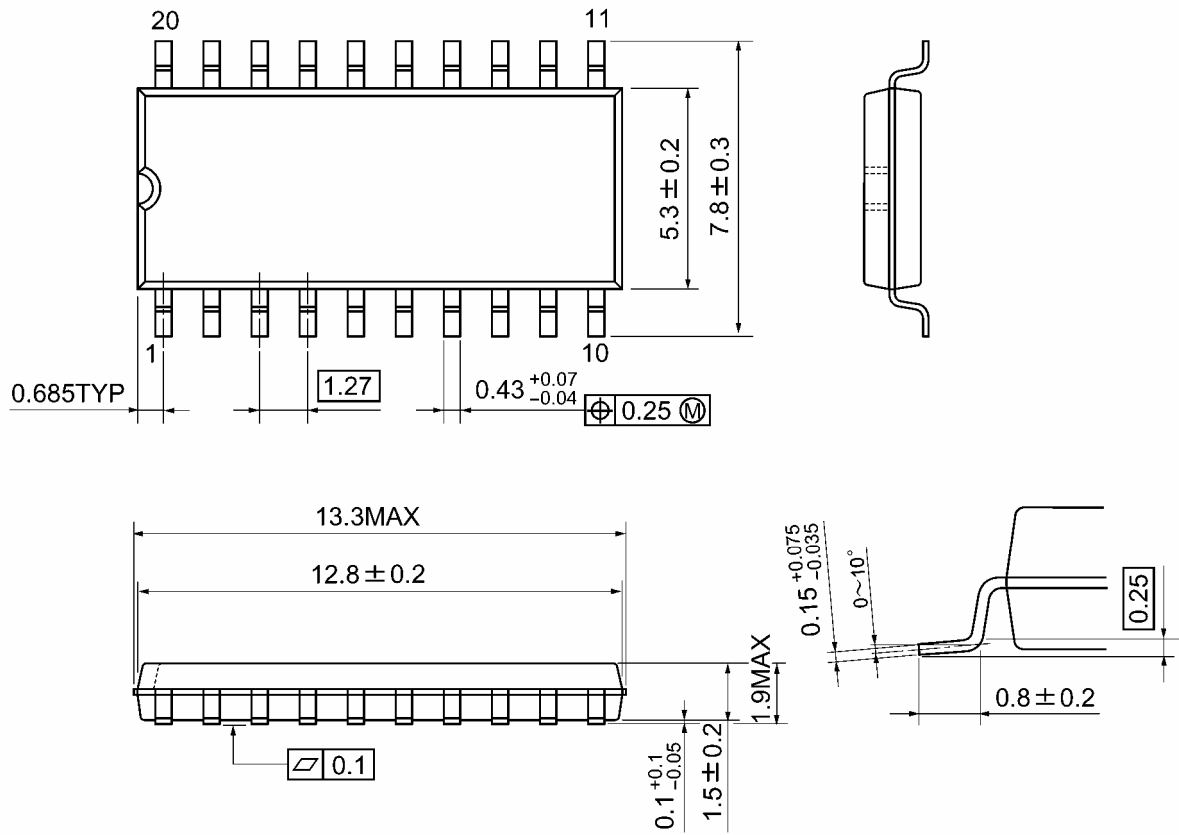


Weight: 1.30 g (typ.)

Package Dimensions

SOP20-P-300-1.27A

Unit: mm



Weight: 0.22 g (typ.)

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20070701-EN GENERAL

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